DMTM Counter System

For the DMTM system four counters are used to measure the period of the ZD1 and ZD2 signals coming from the zero crossing detectors on the mixer and a fifth to measure the phase difference. The period counters are arranged as two pairs for each input with one counter starting as the other stops to provide continuous monitoring of the period between input events. Each event causes the input flip-flop to toggle and the output is sent to a second flip-flop, which synchronizes the event to the 100M clock. The output from the second flip-flop causes one counter to start and the opposite counter to stop.

When the start signal is received the counter is enabled and begins counting the 100M clock pulses. When the external counter overflows it increments TMR1, and when TMR1 overflows an overflow register is incremented. The combination of the 4-bit external counter, 16-bit TMR1, and 8-bit overflow register produce a 28-bit period counter. With a 100M clock the maximum period that can be measured between events is 2.68 seconds with 10us resolution so the common oscillator offset must be greater than 0.38 Hz. Since a 1 Hz offset is typically used the value is displayed as 8-digit BCD so the maximum value is 999.99999ms before overflow. While this is happening the opposite counter is disabled, interrupting the PIC causing it to read the external counter, add the counter value to the PIC internal counter values, store the result, clear the internal and external counters, and set the data ready flag.

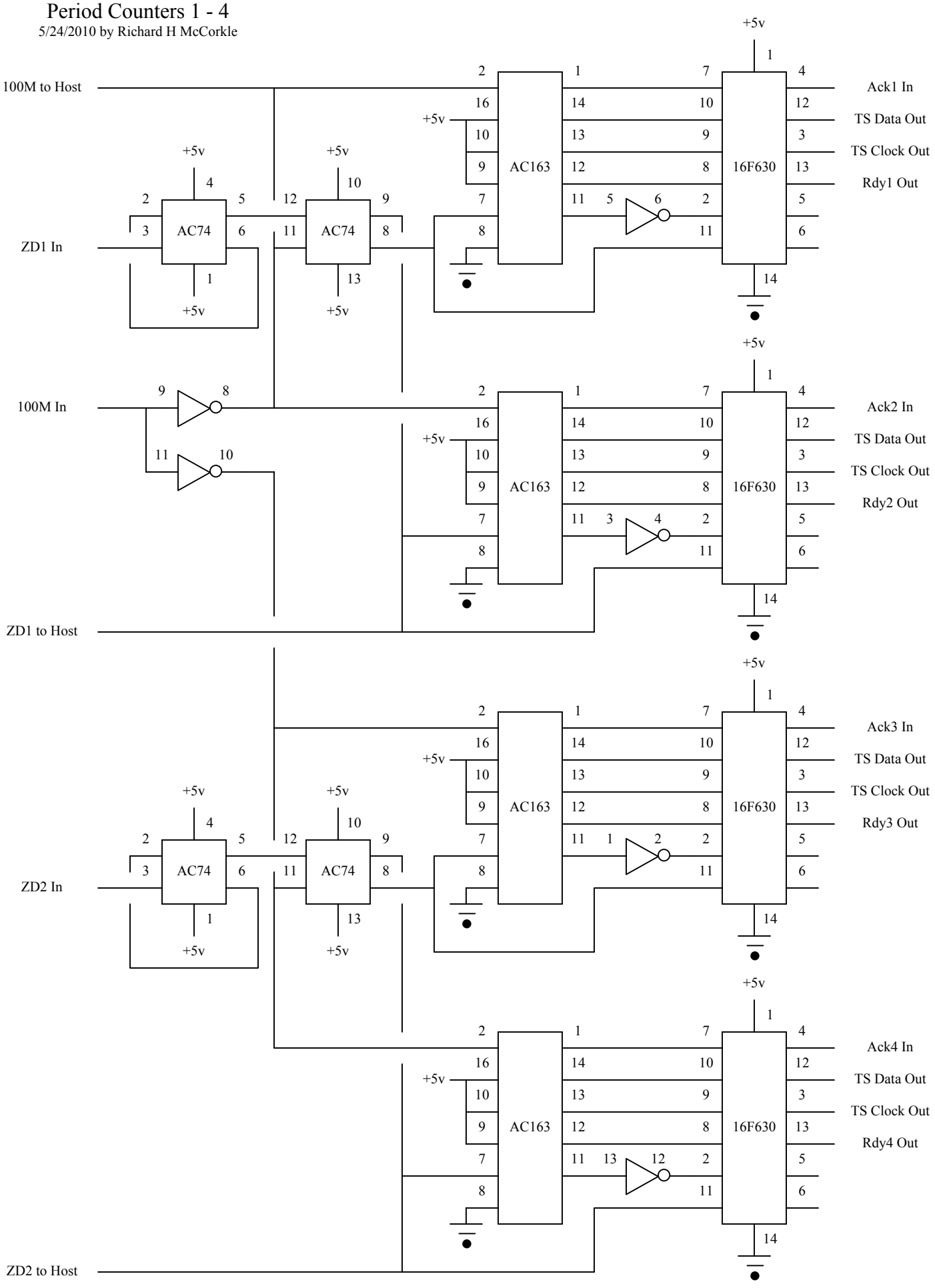
When data ready is detected by the host processor an acknowledge (Ack) signal is sent to the counter. On receipt of the Ack the counter re-defines its clock and data pins from inputs to outputs and sets the data ready line low. This tells the host the counter is ready and will begin sending the data. Once the transmission is complete or an error occurs the counter re-defines its clock and data lines as inputs, freeing the lines for use by the other counters. If the transmission does not complete correctly due to error, the data ready flag is re-set, causing the host to try reading the data again.

To compare the phase of the ZCD outputs the host uses a similar counter and each time the ZD1 output goes high the counter is started. Each time the ZD2 output goes high the counter is stopped and an interrupt is generated. The counter is read and cleared as fast as possible and made ready for the next start. Skipped phase samples can result when the delay between ZD2 and ZD1 rising edges is shorter than the read and reset time so this interrupt is not used to initiate the output update. A limiter can be enabled that inverts the ZD2 signal into the phase counter whenever the value exceeds a user set limit.

The period counter data ready lines are tied to interrupt on change inputs so whenever a data ready pin is set an interrupt occurs. The port is read and stored and the data from any counter with data ready set is read and stored. Any counter that updates and has data ready during the previous read will set one of the inputs again, so the read routine reads the port again at the end of each transfer and loops until all data available has been read. Data from counters 1 and 2 are stored in PB0, and data from counters 3 and 4 are stored in PB1 with the latest data overwriting the previous value. The interrupt bit is cleared, if PB1 has been updated an update flag is set, and background processing resumes. When the update flag is set the background routine clears the flag, converts the latest data to 8-digit BCD, and sends it as PB0 (Sp) PB1 (Sp) Phase (LF/CR) to the serial port at 57.6 KB. This insures no period counter samples are skipped with the latest data reported at each PB1 update.

Period Counters 1 - 4

5/24/2010 by Richard H McCorkle



Host Controller

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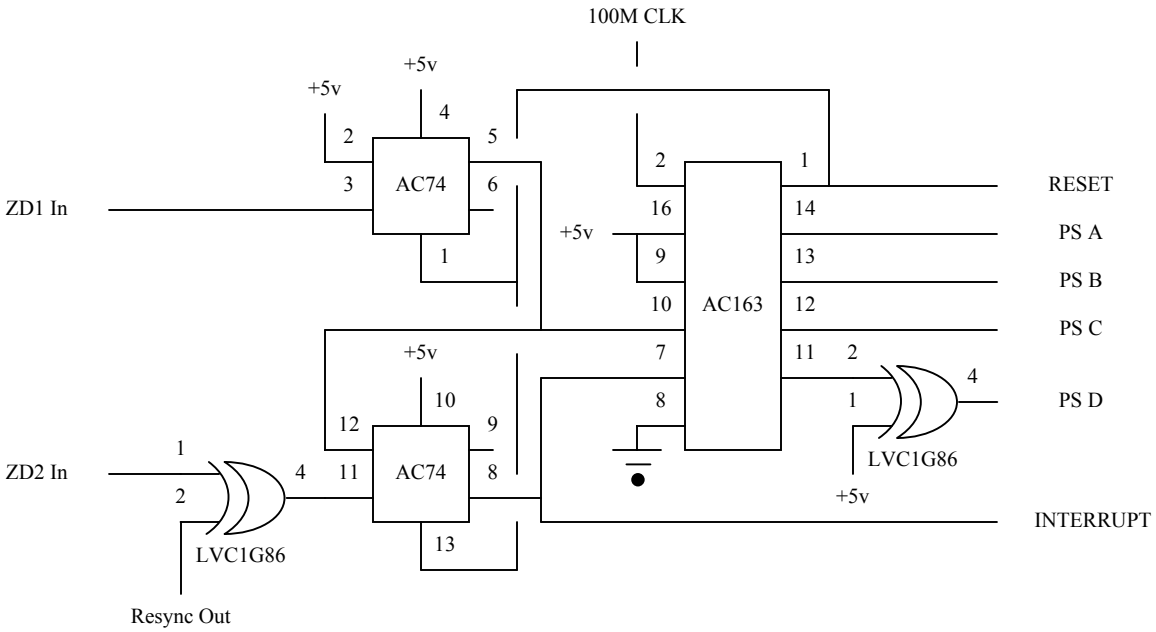

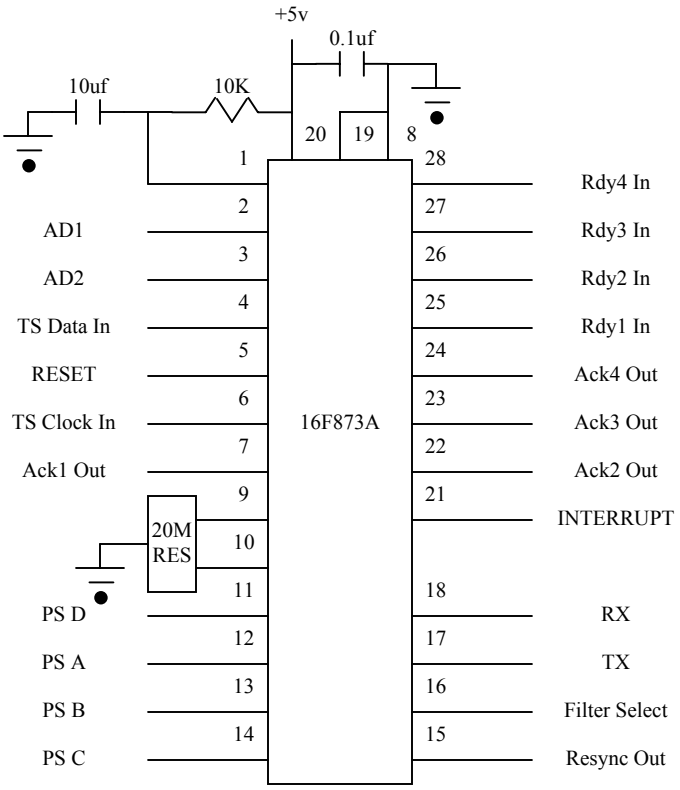

Conditioning Circuitry

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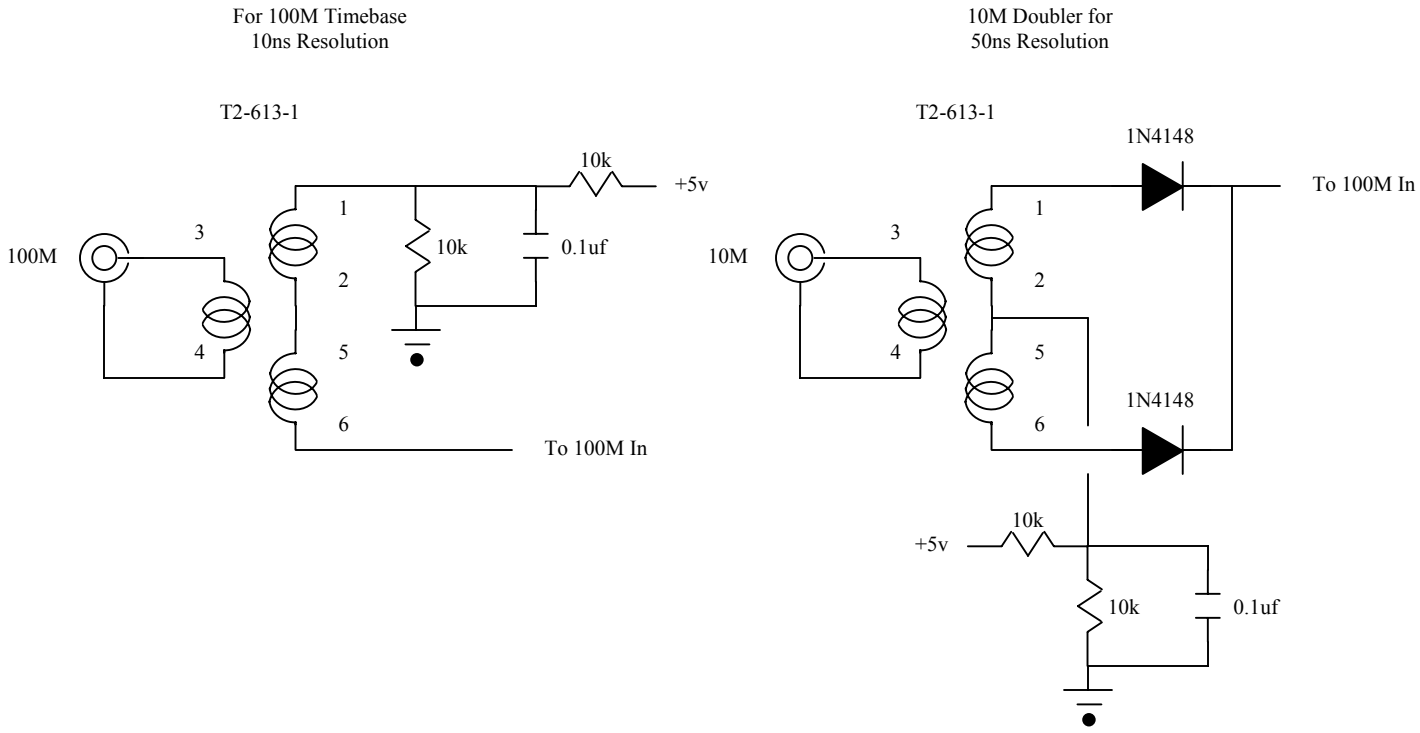

While the counters are designed for a 100M timebase a slower timebase can also be used. Many users will have a 10M signal available, so the clock input includes provisions for doubling the rate to 20M to drive the counters for 50ns resolution. Three pads on the board can be jumpered to allow different clock arrangements as required. The bias network applies a DC voltage to the CMOS clock inverters to lower the signal required to cause them to switch states. The clock bias should be adjusted by component selection as required for the best clock waveform at the outputs of the clock inverters.

Two analog inputs are provided with AD1 typically tied to an LM335 temperature sensor. The controller provides a 0-255 count range from –23.2C to +101.3C at 0.49C per count with this arrangement. The second channel can be used for a second temperature sensor or monitoring other voltages in the system. Provisions are included for displaying the full 10-bit ADC range and adding a dual buffer with feedback divider to increase the gain. Low impedance 0-5v signals can be jumpered directly to the host or a TLV2472CP single supply rail-to-rail op-amp can be installed as a buffer for the inputs with a feedback divider added for higher gain as required.