**Broadband Frequency/Distribution Amplifier** HP E1750A **Pulse Distribution Amplifier** HP E1752A

- Precision clock and 1 pps timing pulse distribution
- Broadband distribution of sinewave signal and pulse trains
- High port-to-port isolation to minimize system crosstalk
- Visual channel-status indicators for fast and easy input and identification of individual input and output channel health
- Built-in AGC for better phase stability and quick setup (no level adjustments)

Module Size-Slots	C-1
Message- or Register-based	RB
HP Foundations Supported	1-5, 13-16
VXI <i>plug&amp;play</i> Frameworks Supported	None

# **(**p) HP E1750A HP E1752A

# **System Frequency Distribution**

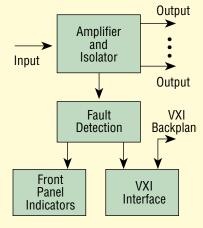
These distribution amplifiers provide up to six buffered outputs for distributing standard clock and other signals in laboratory, factory, and general ATE environments, where key requirements are:

- Broadband sinewave or pulse buffering/distribution
- Distribution of precise clock frequencies
- Distribution of precise 1 pps timing pulses
- High isolation/low crosstalk between output channels
- No level adjustments
- Preservation of input phase and frequency characteristics with changing environment (temperature, humidity, etc.)
- · Channel fault alarm

## **SPECIFICATIONS**

Input Ranges	HP E1750A	HP E1752A
Frequency min	100 kHz	1 pps <sup>(1)</sup>
Frequency max	10 MHz	10 Mpps <sup>(2)</sup>
Level, min	+7 dBm	(3)
Level, max	+19 dBm	(3)
Damage	+27 dBm	-9V, +14 V
Impedance	$50 \Omega$	$50 \Omega$

- (1) May be used with lower pulse repetition rates, with restrictions on duty cycle and fault alarm operation (see manual)
- (2) Mpps = million pulses per second
- (3) Logic LO: ≤0.8 V Logic HI: ≥2.0 V



HP E1750A/E1752A Block Diagram

# E1750A Outputs, 50 $\Omega$ Load

Level	+13 dBm ±1 dB	
Phase noise	<-145 dBc <sup>(4,5)</sup>	
Harmonic distortion	<-45 dBc <sup>(6)</sup>	
Spurious phase modulation	<-80 dBc <sup>(7)</sup>	
Port-to-Port Isolation (open/short loads)		
phase modulation	<-100 dBc	
phase change, peak	<±0.0012°	

(4) Measured 1 kHz from carrier, 1 Hz bw (5) <-142 dBc for 5 MHz,  $\leq$ Frequency in  $\leq$ 10 MHz (6) <-40 dBc for 5 MHz,  $\leq$ Frequency in  $\leq$ 10 MHz (7) Discrete sidebands, 10 Hz to 50 kHz

#### HP E1752A Outputs, 50 $\Omega$ Load

The output pulse (a TTL signal into  $50\Omega$ ) will be a replica of the input pulse, governed by the characteristics outlined under Input Ranges, with the following restrictions:

Rise/fall time < 5 ns Pulse amplitude >3.5 V, typical 22 ns, typical Propagation Delay Jitter <1 ns rms

#### **Power Requirements**

See the Module Power and Cooling Information Table in Appendix A-1.



#### **For More Information**

HP E1750A/E1752A Brochure HP Pub no. 5091-7546 EUS

## **Ordering Information**



