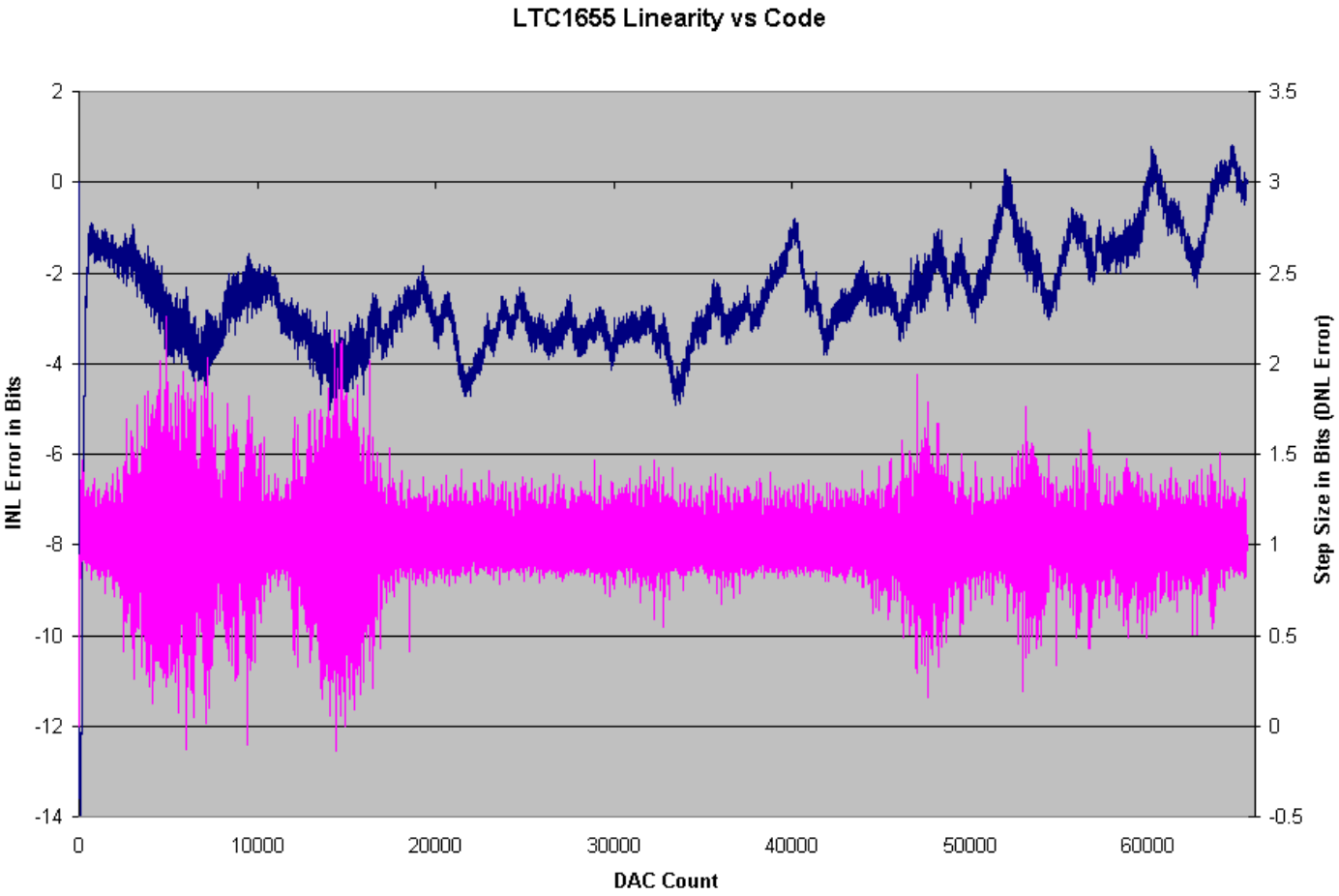
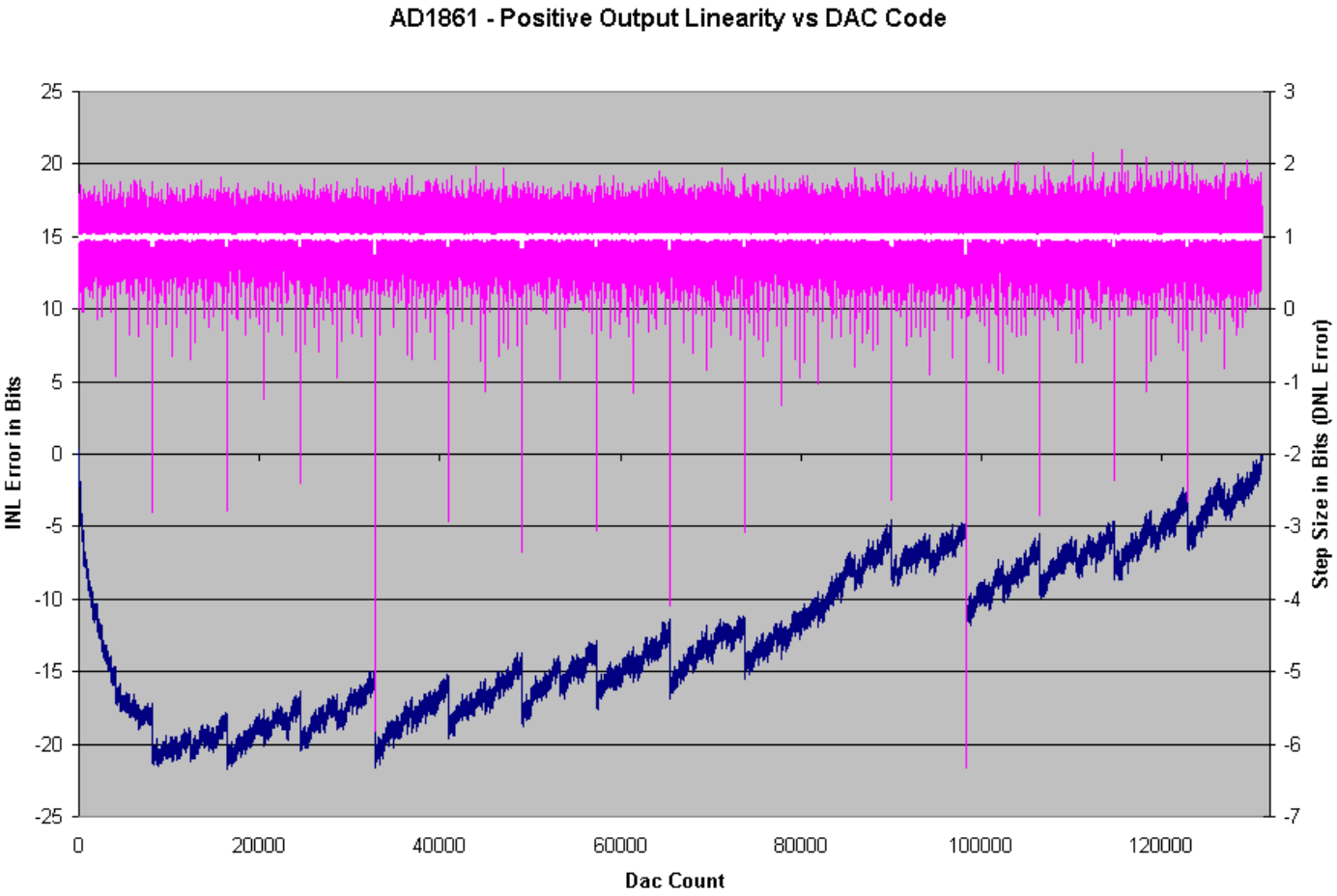
Initial Comparison of the AD1861 and LTC1655 DACs

The LTC1655 is a modern 16-bit DAC being evaluated for use in a discipline controller. The zero offset is specified at code 200 as +/- 3mv with a specified gain error of +/- 16 LSB at full scale. The internal reference is specified as 2.048v +/- 12mv, translating to a typical output of 4.0959375v +/- 1mv with an LSB resolution of 62.5uv, a minimum output of 4.071v, and a maximum output of 4.121v. The test data shows an output at code 200 of 12.293mv vs. the ideal 12.5mv so the output is low by 207uv, but is well within the +/- 3mv offset specification. The maximum output was 4.087754v, so the output was greater than the minimum specified full-scale output of 4.071v and the maximum error from nominal was 0.5mv so it meets the gain specification of +/- 1mv across the output span.

The DNL is specified as +/- 1 LSB from codes 128 thru 65535 and the INL is specified as +/- 20 LSB. The worst-case step change between any two adjacent codes between codes 128 and 65536 was +1.26 LSB and –1.13 LSB so technically this exceeds the +/- 1 LSB DNL specification, but remains below +/- 1.3 LSB in the device tested. The worst case INL error is –15.42 bits at code 75 so the device tested meets the INL specification of +/- 20 LSB, with a typical INL error between +0.72 bits and -4.75 bits from codes 334 to 65535.



The LTC2400 ADC used during the test requires inputs between -0.625v and 5.625v so testing the older AD1861 required separate tests for the positive and negative portions of its –3v to +3v output span. Since the negative portion could not be tested directly and the results would be influenced by the inverter gain and temperature stability, the results presented below are from testing the positive portion of the DAC span directly into the ADC.



The specifications for the AD1861 give the Mid Scale Offset as +/- 10mv with an Output Span of +/- 2.88v to +/- 3.12v. The DNL is +/- 0.001% of FSR with a Monotonicity of 15 bits. The Gain Error is +/- 1% with a Bipolar Zero Drift of +/- 4 PPM/C of FSR and a Total Drift of +/- 25 PPM/C of FSR. The tested span is 262143 counts over a +/- 2.997v or 5.994v range so the device meets the specified +/- 2.88v to +/- 3.12v output span. The mid-scale offset at code 0 was -2.698mv and is within the +/- 10mv mid-scale offset specification. The DNL is specified as +/-0.001% of span equaling +/- 60uv or +/- 2.6 bits and over the majority of the codes it is within +/- 1 bit, but there are exceptions, primarily at the 4k boundaries. Here the specified monotonicity of 15 bits enters in allowing a maximum +/- 8-code voltage deviation between adjacent steps.

The maximum adjacent code deviation from nominal was +2.19 bits to – 6.32 bits so the device meets a monotonicity of 15 bits. The INL is not specified for the AD1861 but when the data was corrected for zero offset and span errors the worst-case INL error was -21.56 bits in the device tested. The worst-case errors from nominal occur near the zero

crossing point (outputs within +/- 110uv of 0v) with the errors from codes 105-114 exceeding 50% of nominal and a worst-case error at code 109 where the actual output was -68.9uv and should have been -4.4uv, an error of -64.5uv or 1455% of the nominal output value. The testing was done without the MSB adjustment circuit shown in the AD1861 spec sheet resulting in relatively large code errors at outputs between –110uv and +110uv that may be correctable with the adjustment circuit. The mid-scale polarity transition should not be used as the optimum EFC at setpoint in a GPSDO without adding the MSB adjustment circuit due to the large gain errors as the polarity reverses thru 0v.

It was interesting to note that there are codes that result in drastic step glitches in the output. These glitches occur exactly on 4k-boundary codes and are of short duration, returning to a normal level within 2 codes. The average step increment is 22.883uv but there are numerous codes that result in no change, twice the expected change, or cause the output to go negative instead of positive as the code increases. At 4096 code intervals the output drops typically 1-2 bits in level with greater differences at 8192 code intervals of typically 2-3 bits. At 32k the level drops 5.82 bits, at 64k the level drops 4.08 bits, and at 96k the most extreme drop is 6.32 bits. These 4k-boundary errors are probably the reason the manufacturer only specifies 15-bit monotonicity for this 18-bit DAC.