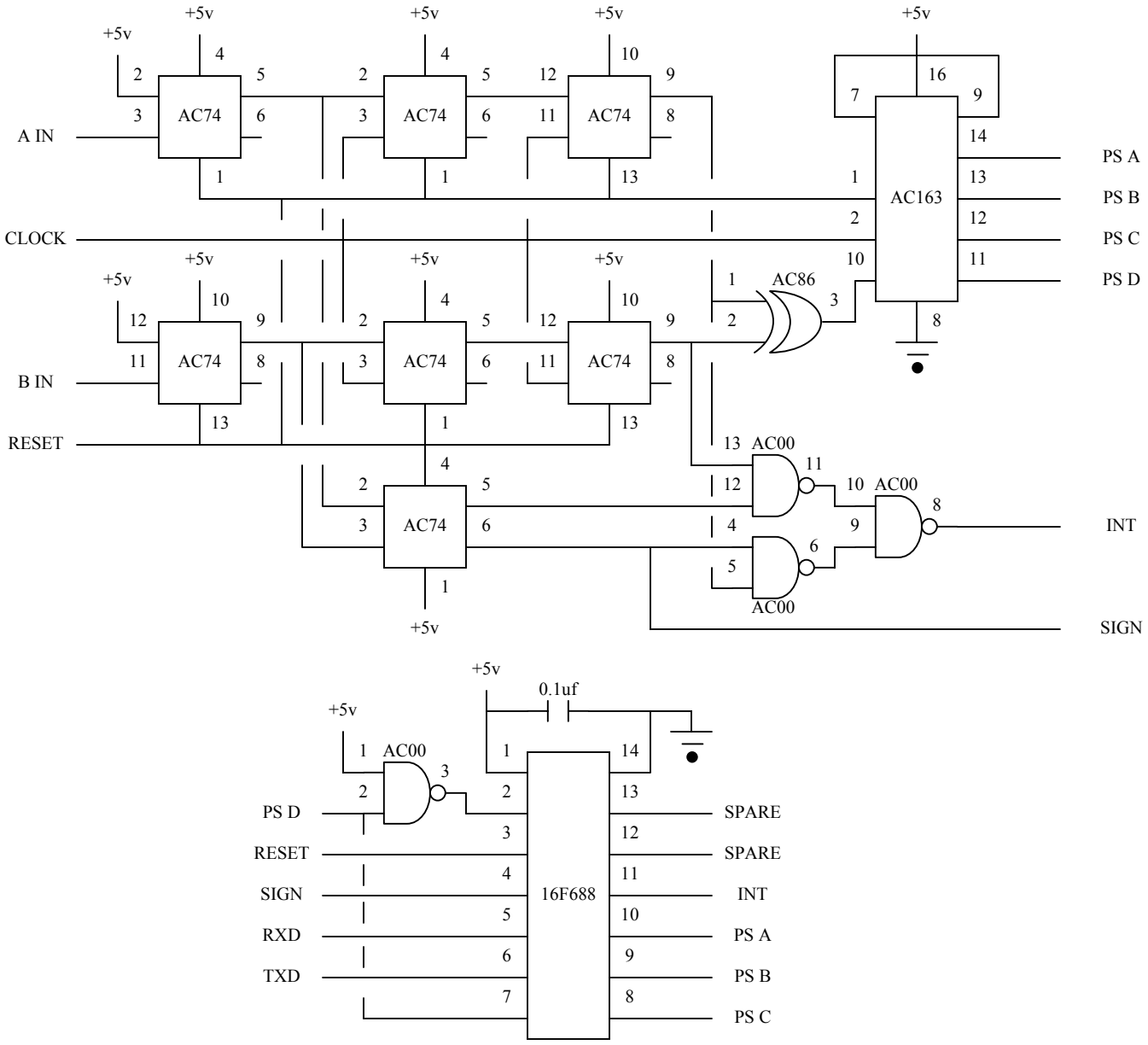
PICTIC+ With Start Channel Detection for DMTM



The synchronizers cause a 2-clock delay before counter start allowing time to switch the interrupt and set the sign bit prior to counter start. Normally A would be start so we start the channel determination F/F in the set state at reset. The sign bit would be low and the B synchronizer output would provide the interrupt if the A channel input F/F is high when the B channel input F/F goes high. At reset both synchronizer outputs are low so a constant low will be presented at the INT line during the switch. If B occurs first the low on the D input from the A input F/F resets the channel F/F setting the sign bit and selecting the A synchronizer output as the interrupt. The input F/Fs should be in a common package to equalize the propagation times for best results.