2. Connect oscilloscope to the gate (metal case) of FET Q6.

3. Adjust C37 for maximum signal on oscilloscope display.

4. Connect oscilloscope to collector of transistor Q7.

5. Adjust capacitor C45 and inductor L13 for maximum 60 MHz signal display on the oscilloscope. If the maximum is not obtained with the adjustment of L13, try a different setting of C30. Note the amplitude of the oscilloscope display. It should indicate greater than 6 Vp-p.

6. Disconnect oscilloscope from collector of transistor Q7.

g. ALIGNMENT OF OUTPUT AMPLIFIER STAGE

NOTE

In the following procedure, the output amplifier should be adjusted for maximum RF output at minimum Q12 dc collector current. Monitor the +20 Volt dc current by either measuring current with an ammeter or by measuring the dc voltage drop across inductor L16.

1. Connect RF voltmeter to J8 (if not already connected).

2. Connect dc voltmeter to TP2.

3. Adjust C50, C52, C60, and C54 to get maximum RF voltmeter reading at J8.

4. Adjust C60 for minimum dc current indication.

5. Readjust C37, L13, C45, and C54 for maximum dc voltage at TP2.

6. Adjust C50 and C52 for maximum RF voltage at J8.

7. Repeat steps 4 and 6 until RF output (as measured at J8) is between +3.2 and +3.6 Volts rms. If specified output is measured at J8, further adjustment of C50 and C52 is NOT required. Check the mechanical setting of capacitor C52. If C52 is set close to its maximum capacitance setting, change capacitor C56 to a higher capacitance value. Conversely, if C52 is set close to its minimum capacitance setting, change C56 to a lower capacitance value. Select capacitors from A3 parts list found in Section VI of this manual. If it was necessary to change C56, repeat steps 3 through 7.

8. Remove 20k Ohm resistor installed earlier in R45 location and reinstall original resistor in its place.

9. Readjust C60 for minimum dc current indication.

10. Readjust C37, L13, C45, and C54 for maximum AGC voltage indication and optimum RF output power. The AGC voltage should be greater than +4.5 dc Volts and the RF voltage reading at J8 should fall between +2.7 and 3.0 Volts rms. If measured voltages are within specifications, continue with step 12. If either the AGC dc voltage or the RF output voltage fails to meet its specification, continue with step 11.

11. Change the resistance value of R45 until both the AGC dc (TP2) and RF rms voltages are in spec. As the resistance of R45 is reduced, the RF power output is decreased and the AGC voltage is increased. Select R45 so that the RF output at J8 is approximately 2.85 Volts rms. Use resistor R45 values listed in Section VI of this manual. Return to step 9 after EACH resistor value change.

12. To check the AGC feedback circuit, connect TP2 to chassis ground. RF voltage at output connector J8 should increase to a value greater than 3.0 Volts rms. Remove short to ground.

13. The A3 Multiplier alignment procedure is now complete. Remove test cable(s), 50-ohm load(s), and all test equipment from the A3 assembly.

14. Replace shield cover on A3 assembly.

15. Install A3 assembly in HP 5065A chassis and reconnect all cabling.

h. A3 MATCHING NETWORK ADJUSTMENTS.

The matching network adjustments are as follows:

R53 .. This control sets bias for the step-recovery diode located in the A12 Assembly.

C55, C61, and L22 . These adjustments match the multiplier output to the load presented by the step-recovery diode circuit located in the A12 Assembly.

The matching network adjustment must be aligned with the A3 Multiplier installed in the system. See paragraph 5-25, RF ALIGNMENT under LOOP ALIGNMENT PROCEDURE for adjustment instructions.

MODULE REPLACEMENT

When replacing the A3 Assembly after repair or when a new A3 Assembly is installed, the instrument should be completely realigned per paragraph 5-19, LOOP ALIGNMENT PROCEDURE.